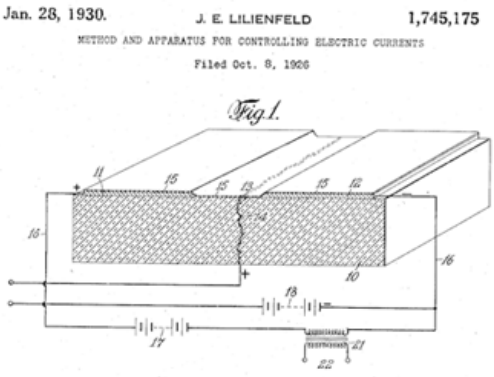
Chapter 8:Field Effect Transistors (FET's)

The FET

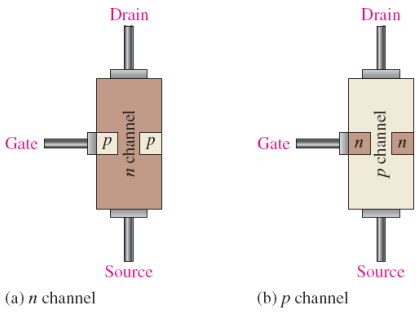
- The idea for a field-effect transistor (FET) was first proposed by Julius Lilienthal, a physicist and inventor. In 1930 he was granted a U.S. patent for the device.

- His ideas were later refined and developed into the FET. Materials were not available at the time to build his device. A practical FET was not constructed until the 1950's. Today FETs are the most widely used components in integrated circuits.



8-1: The Junction Field Effect Transistor (JFET)
Basic Structure

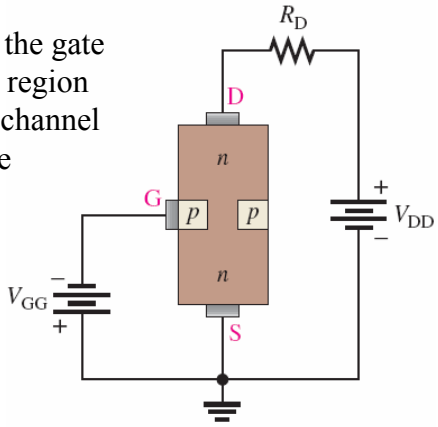
- The **JFET** (junction field-effect transistor) is a type of FET that operates with a reverse-biased *pn* junction to control current in a channel.
- JFETs has two categories, *n* channel or *p* channel.
- For *n*-channel JFET shown; the **drain (D)** is at the upper end, and the **source (D)** is at the lower end. Two *p*-type regions are diffused in the *n*-type material to form a **channel,** and both *p*-type regions are connected to the **gate (G)** lead.
- for p-channel, the gate is connected to n-type regions forming the channel into the p-type material



basic structure of the two types of JFET.

8-1: The Junction Field Effect Transistor (JFET)
Basic Operation

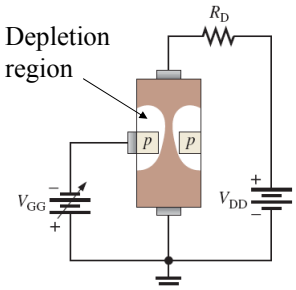
- Biasing of JFET is shown in the figure
  - V_{DD} provide drain-to-source voltage → current flow from drain to source
  - V_{GG} sets the reverse bias between the gate and the source → sets the depletion region along the pn junction → restricting channel width → increase channel resistance



8-1: The Junction Field Effect Transistor (JFET)

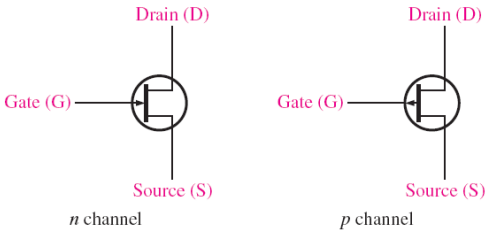
Basic Operation

■ By varying the gate voltage (V_{GG}) →increasing –ve voltage between G and S → varying the channel width → controlling the amount of drain current (I_D); As V_{GG} increase → depletion region increase → channel decrease → higher resistance → lower current



JFET biased for conduction

■ The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in the adjacent figure; the arrow on the gate points "in" for *n* channel and "out" for *p* channel.



n channel *p* channel

8-2: JFET Characteristics And Parameters

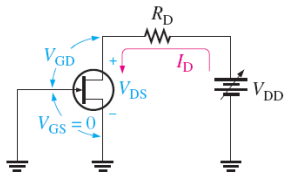
The JFET operates as a voltage-controlled, constant-current device

Drain characteristic curve

■ If you set the gate-to-source voltage to be zero ($V_{GS} = 0$) by shorting gate-to-source as shown → as V_{DD} increase, I_D increase and thus V_{DS} increase (***Ohmic region*** between A and B → constant R between D and G).

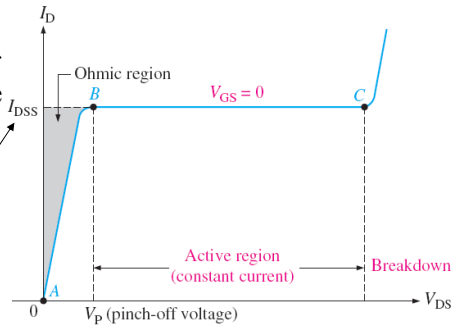
■ At point B (at V_{DS} = ***pinch-off-voltage*** - V_p) → current I_D becomes constant (active region between B and C); this is due to reverse bias voltage from gate-to-drain V_{GD} which prevent any further increase in I_D with increasing V_{DS}

■ at point C where ID rapidly increase → ***breakdown region*** → JFET may damage



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

max. drain current for given JFET. It is usually specified at $V_{GS} = 0$

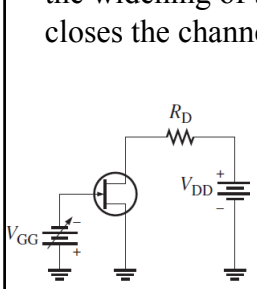


(b) Drain characteristic

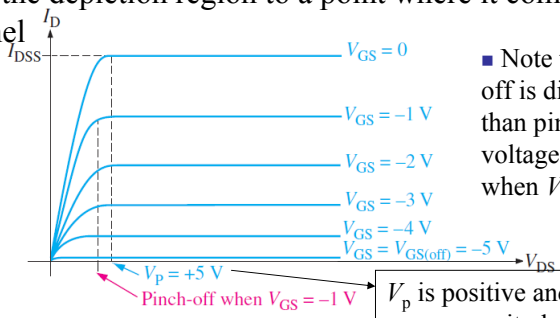
8-2: JFET Characteristics And Parameters

Drain characteristic curve

- When V_{GS} is set to different values, the relationship between V_{DS} and I_D develops a family of characteristic curves for the device (figure below).
- The figure shows the more negative V_{GS} is, the smaller I_D (constant smaller current begins at ***pinch-off***) becomes in the active region.
- When V_{GS} has a sufficiently large negative value, I_D is reduced to zero → $V_{GS} = V_{GS(off)}$ (***cut off voltage***). This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel



V_{GS} is set different by adjusting V_{GG}



Family of drain characteristic curves

- Note that pinch off is different than pinch off voltage measured when $V_{GS} = 0$

V_p is positive and has the same magnitude as V_{GS}(off).

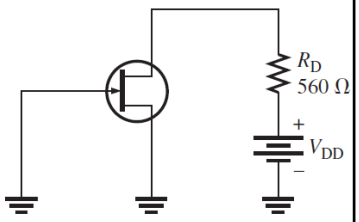
8-2: JFET Characteristics And Parameters

Example:

For the JFET in Figure 8–11, $V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA. Determine the *minimum* value of V_{DD} required to put the device in the constant-current region of operation when $V_{GS} = 0$ V. If V_{DD} is increased to 15 V, what is the drain current?

$V_{GS(off)} = -4\text{ V} \longrightarrow V_P = V_{DS} = 4\text{ V}$

from KVL $V_{DD} = V_{DS} + V_{R_D}$



$$\rightarrow V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$
$$= 4\text{ V} + 6.72\text{ V} = \mathbf{10.7\text{ V}}$$

If V_{DD} increases to 15 V → V_{DS} will increase. But I_D will remain the same

8-2: JFET Characteristics And Parameters

JFET Universal Transfer Characteristic

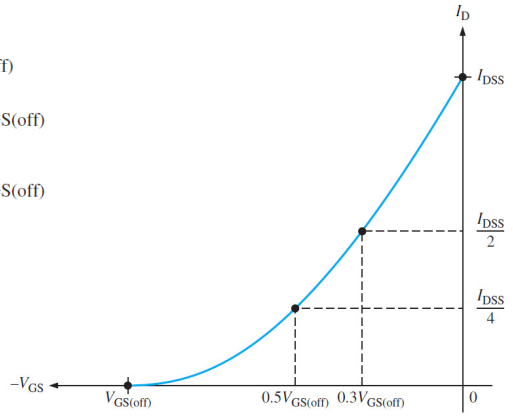
- Because VGS control the drain current I_D → a plot of the output current (I_D) to the input voltage (V_{GS}), called the transfer or transconductance curve, can be drawn:

$I_D = 0 \longrightarrow V_{GS} = V_{GS(off)}$

$I_D = \frac{I_{DSS}}{4} \longrightarrow V_{GS} = 0.5V_{GS(off)}$

$I_D = \frac{I_{DSS}}{2} \longrightarrow V_{GS} = 0.3V_{GS(off)}$

$I_D = I_{DSS} \longrightarrow V_{GS} = 0$



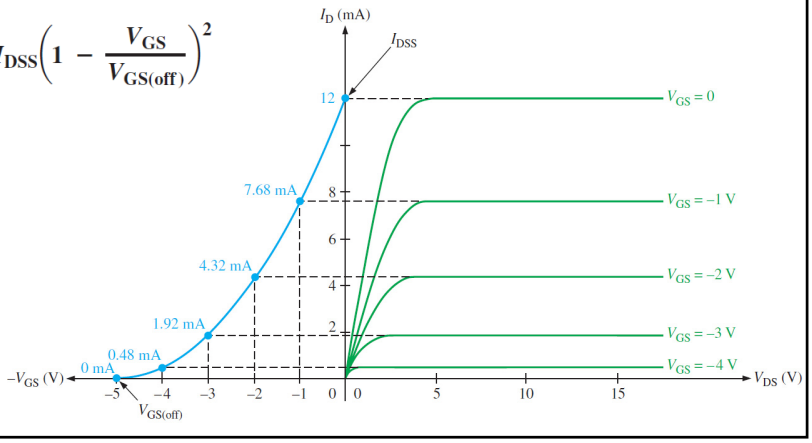
general transfer characteristic curve between V_{GS} and I_D

8-2: JFET Characteristics And Parameters

JFET Universal Transfer Characteristic

- The transfer characteristic curve can also be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off (at different constant drain currents).
- for different V_{GS}, JFET I_D's can be mathematically expressed by

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



8-2: JFET Characteristics And Parameters

Example:

The partial datasheet for a 2N5459 JFET indicates that typically $I_{DSS} = 9$ mA and $V_{GS(off)} = -8$ V (maximum). Using these values, determine the drain current for $V_{GS} = 0$ V, -1 V, and -4 V.

For $V_{GS} = 0$ V ⟶ $I_D = I_{DSS} = \mathbf{9\ mA}$

For $V_{GS} = -1$ V, use Equation

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$
$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = \mathbf{6.89\ mA}$$

For $V_{GS} = -4$ V,

$$I_D \cong (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = \mathbf{2.25\ mA}$$

8-2: JFET Characteristics And Parameters

JFET Forward Transconductance

- The transconductance (transfer conductance), g_m (or g_{fs} or y_{fs}- forward transfer admittance), is an important factor in determining the voltage gain of a FET amplifier as you will see later. g_m is the ratio of a change in output current (ΔI_D) to a change in the input voltage (ΔV_{GS}):

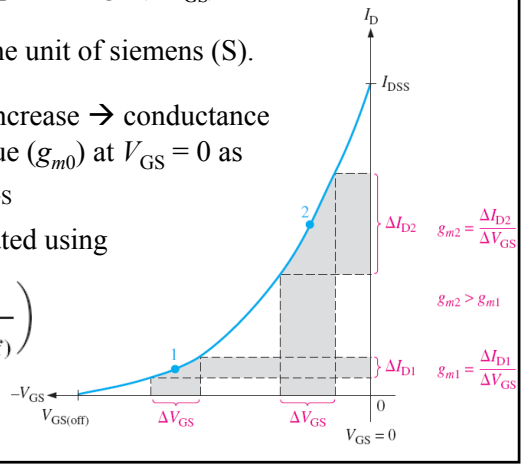
⟶ $$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$ has the unit of siemens (S).

- As V_{GS} increase → resistance increase → conductance decrease → g_m has its highest value (g_{m0}) at $V_{GS} = 0$ as shown in the figure for given ΔV_{GS}

- At given V_{GS}, g_m can be calculated using

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

where $$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$



8-2: JFET Characteristics And Parameters

JFET Forward Transconductance: Example:

for a 2N5457 JFET: typically, I_{DSS} = 3.0 mA, $V_{GS(off)}$ = -6V maximum, and $g_{fs(max)}$ = 5000 mS. Using these values, determine the forward transconductance for V_{GS} = -4V, and find I_D at this point.

$g_{m0} = g_{fs(max)} = 5000\ \mu S.$

$$\rightarrow g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = (5000\ \mu S)\left(1 - \frac{-4\ V}{-6\ V}\right) = \mathbf{1667\ \mu S}$$

to calculate I_D at $V_{GS} = -4$ V.

$$\rightarrow I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (3.0\ mA)\left(1 - \frac{-4\ V}{-6\ V}\right)^2 = \mathbf{333\ \mu A}$$

8-2: JFET Characteristics And Parameters

Input Resistance and Capacitance

- Input resistance (R_{IN}) of the JFET is the resistance of the reverse-biased gate-source junction → At given V_{GS} with reverse gate-source current I_{GSS}

$$\rightarrow R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$ See Example 8-5

- For JFET, R_{IN} is usually very high and decrease with temperature, T, since I_{GSS} increases with T.
- The input capacitance, C_{iss}, is a result of the JFET operating with a reverse-biased (depletion layer act as a capacitor in reverse biase)

AC Drain-to-Source Resistance

- above the pinch off, I_D is relatively constant; Only small change in I_D occurs over a wide range of V_{DS} → we have ac drain-to-source resistance

$$r'_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

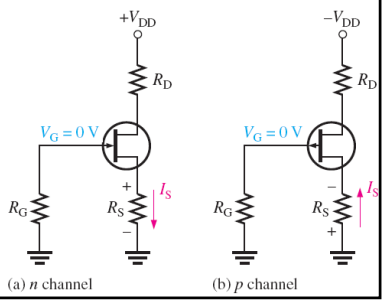
Datasheets specify this parameter as output conductance, g_{os}, or output admittance, y_{os}, for V_{GS} = 0 V.

8-3: JFET Biasing

We can use the JFET parameters discussed to properly bias the JFET by dc voltage (V_{GS}) and determine a proper Q-point. Three types of bias are self-bias, voltage-divider bias, and current-source bias.

a - Self-Bias

- JFET must be operated such that the gate-source junction is always reverse-biased. →-ve V_{GS} for an *n*-channel JFET and a +ve V_{GS} for a *p*-channel JFET. This can be achieved using the self-bias arrangements shown
- Self-bias is simple and effective, so it is the most common biasing method for JFETs. With self bias, the gate is essentially at 0 V.
- For ***n-channel***, R_S is added to makes the source positive with respect to ground (I_S produce a voltage drop across R_S)→ R_S develops the necessary reverse bias that forces the gate voltage ($V_G = 0$; $I_G = 0$) to be less than the source.
- the inverse is for p-channel



8-3: JFET Biasing

a - Self-Bias: Setting the Q-point

- The gate to source voltage is

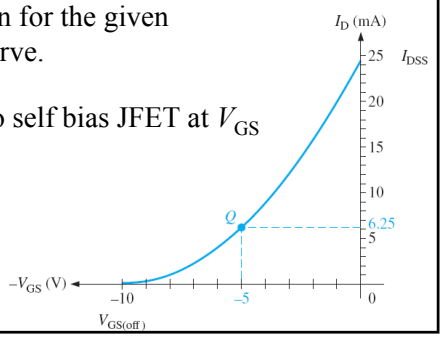
$$V_{GS} = V_G - V_S = 0 - I_S R_S = -I_S R_S$$

$$\longrightarrow V_{GS} = -I_D R_S \qquad \text{Since } I_S = I_G + I_D = 0 + I_D = I_D$$

Reverse current; ideally = 0

$$\Rightarrow R_S = \left|\frac{V_{GS}}{I_D}\right|$$

Which can be found for certain Q-point (certain V_{GS} and I_D) as shown for the given transconductance curve.



For the shown curve, the value of R_S to self bias JFET at V_{GS} = -5V is

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$$

8-3: JFET Biasing

a - Self-Bias: Setting the Q-point

■ It is usually preferable to bias the JFET near the mid point of it's transfer curve (at $I_D = I_{DSS}/2$ and $V_D = V_{DD}/2$) → midpoint bias allows the maximum amount of drain current swing between I_{DSS} and 0 when there is an ac signal applied to JFET.

Using $$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

and substitute for $I_D = I_{DSS}/2$ → $V_{GS} = V_{GS(off)}/3.4 \approx 0.3V_{GS(off)}$

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop. →

$$V_D = V_{DD} - I_D R_D$$
$$I_D R_D = V_{DD} - V_D$$
$$R_D = \frac{V_{DD} - V_D}{I_D}$$

8-3: JFET Biasing

a - Self-Bias: Setting the Q-point: Example

select resistor values for R_D and R_S in Figure to set up an approximate midpoint bias.

For midpoint bias,

$$I_D \cong \frac{I_{DSS}}{2} = \frac{1.0\text{ mA}}{2} = 0.5\text{ mA}$$

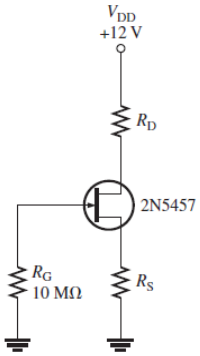
and

$$V_{GS} \cong \frac{V_{GS(off)}}{3.4} = \frac{-0.5\text{ V}}{3.4} = -147\text{ mV}$$

Then

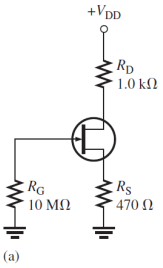
$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{147\text{ mV}}{0.5\text{ mA}} = \mathbf{294\ \Omega}$$

$$V_D = V_{DD} - I_D R_D$$
$$I_D R_D = V_{DD} - V_D$$
$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12\text{ V} - 6\text{ V}}{0.5\text{ mA}} = \mathbf{12\ k\Omega}$$



8-3: JFET Biasing

a - Self-Bias: Setting the Q-point



■ Indeed, for a given circuit, you can use the transfer curve of a JFET and certain parameters to determine the Q-point (I_D and V_{GS}) of a self-biased circuit. For shown circuit with shown transfer curve, the Q-point can be determined by:

a) Draw the transfer curve

b) calculate V_{GS} when I_D is zero.

→ $V_{GS} = -I_D R_S = (0)(470\ \Omega) = 0\ \text{V}$

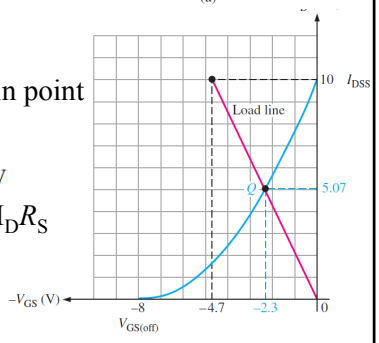
→ Setting the first point I_D=0 and V_{GS} = 0 - origin point

(c) calculate V_{GS} when $I_D = I_{DSS}$

$V_{GS} = -I_D R_S = -(10\ \text{mA})(470\ \Omega) = -4.7\ \text{V}$

→ Setting the second point $I_D = I_{DSS}$ and $V_{GS} = -I_D R_S$

(d) Connect between the two points on the curve by a line (dc load line)→ the intercept of the line with transfer curve is the Q-point

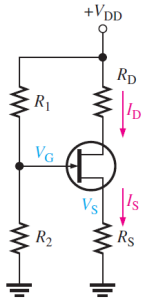


■ stability of Q-point can be increased by increasing R_S and connect it to a negative bias voltage → dual supply bias

8-3: JFET Biasing

b - Voltage-Divider Bias and the Q-point

Voltage-divider biasing shown is a combination of a voltage-divider and a source resistor to keep the source more positive than the gate → gate-source junction is reverse biased. The dc voltages (determining the Q-point) can be found by as followed:



An *n*-channel JFET with voltage-divider bias ($I_S = I_D$).

Source voltage is $V_S = I_D R_S$

and by voltage divider, gate voltage is $V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$

The gate-source voltage then is $V_{GS} = V_G - V_S$

→ $V_S = V_G - V_{GS}$

The drain current $I_D = \frac{V_S}{R_S}$ or $I_D = \frac{V_G - V_{GS}}{R_S}$ Note that $I_D = I_S$

Drain current can also be calculated if you know V_D → $I_D = \frac{V_{DD} - V_D}{R_D}$

8-3: JFET Biasing

b - Voltage-Divider Bias: Example

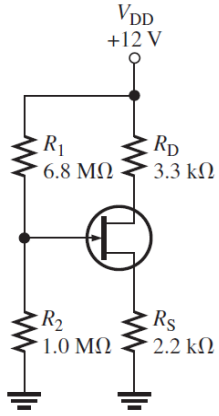
Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure 8–24, given that for this particular JFET the parameter values are such that $V_D \cong 7$ V.

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = \mathbf{1.52\text{ mA}}$$

$$V_S = I_D R_S = (1.52\text{ mA})(2.2\text{ k}\Omega) = 3.34\text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{1.0\text{ M}\Omega}{7.8\text{ M}\Omega}\right)12\text{ V} = 1.54\text{ V}$$

$$\rightarrow\ V_{GS} = V_G - V_S = 1.54\text{ V} - 3.34\text{ V} = \mathbf{-1.8\text{ V}}$$



■ In this example, If V_D had not been given, the Q-point values could not have been found without the transfer characteristic curve.

8-3: JFET Biasing

b - Voltage-Divider Bias and the Q-point

■ Q-point can also be graphically determine the Q-point of a circuit on the transfer characteristic curve as followed:

a) Draw the transfer curve

b) calculate V_{GS} when I_D is zero. ⟶ $V_S = I_D R_S = (0)R_S = 0\text{ V}$

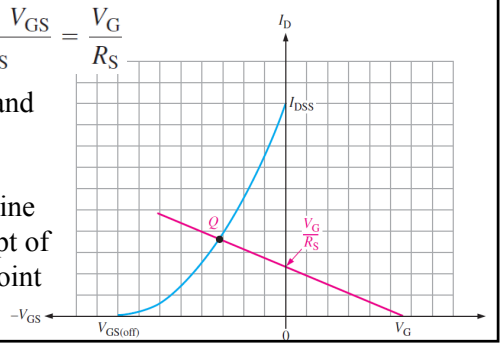
$$V_{GS} = V_G - V_S = V_G - 0\text{ V} = V_G$$

⟶ Setting the first point $I_D = 0$ and $V_{GS} = V_G$

c) For $V_{GS} = 0$ ⟶ $I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$

⟶ Setting the second point $V_{GS} = 0$ and $I_D = V_G/R_S$

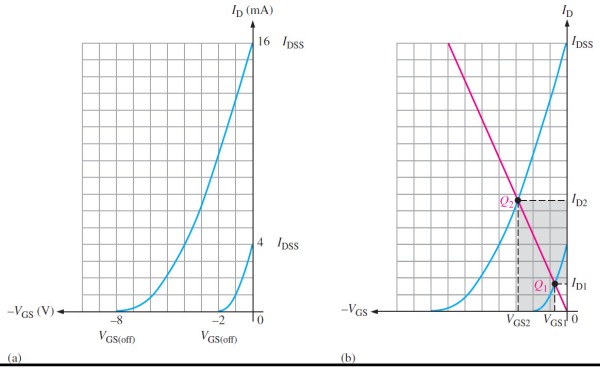
(d) Draw the voltage divider dc load line between the two points → the intercept of the line with transfer curve is the Q-point



8-3: JFET Biasing

c – Current Source Bias –stability of Q-point

- Unfortunately, the transfer characteristic of a JFET can differ very much from one device to another of ***the same type.***
- For example for two devices of 2N5459 JFET, you may have two different I_{DSS} and $V_{GS(off)}$ as shown on self biase transfere curve → the Q-point could be any value between the minimum Q_1 and maximum Q_2 →not fixed I_D and V_{GS} for given device number → since ID is not stable means the Q-point is not stable.



8-3: JFET Biasing

c – Current Source Bias –stability of Q-point

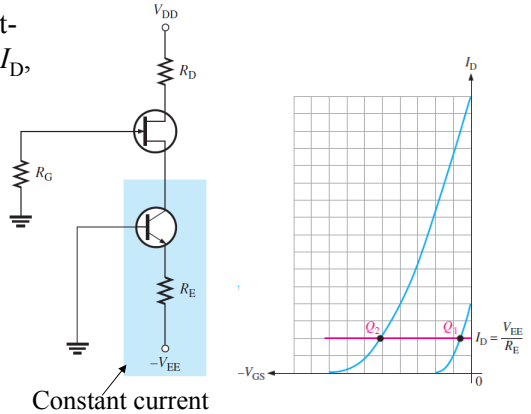
- Indeed, stability of Q-point in self biased JFET can be increased by providing a given constant I_D through adding a constant current source in series with JFET as shown
- The current-source can be either a BJT or another FET. With current-source biasing, the drain current, I_D, is constant ≈ I_E and is essentially independent of V_{GS}.

The emitter current

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \cong \frac{V_{EE}}{R_E}$$

but $I_E \cong I_D$,

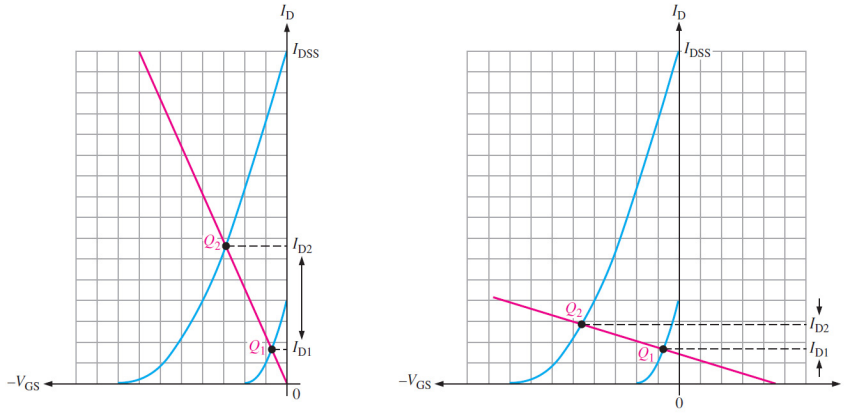
$$\longrightarrow \quad I_D \cong \frac{V_{EE}}{R_E}$$



8-3: JFET Biasing

c – Current Source Bias –stability of Q-point

■ Also the Q-point in voltage divider bias for devices of same type is consider to be more stable because the slope of voltage divider dc load line is less than that in self bias JFET as shown. But still we can add constant current source to guarantee the stability



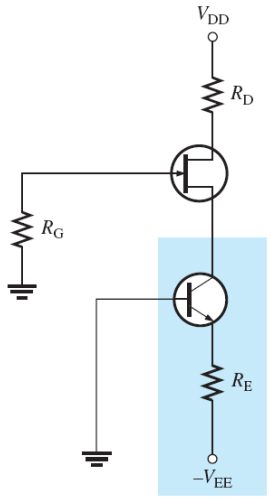
8-3: JFET Biasing

c – Current Source Bias: Example

A current-source bias circuit like Figure 8–29 has the following values: $V_{DD} = 9$ V, $V_{EE} = -6$ V, and $R_G = 10$ MΩ. To produce a 10 mA drain current and a 5 V drain voltage, determine the values of R_E and R_D.

$$R_E = \frac{V_{EE}}{I_D} = \frac{6\text{ V}}{10\text{ mA}} = \mathbf{600\ \Omega}$$

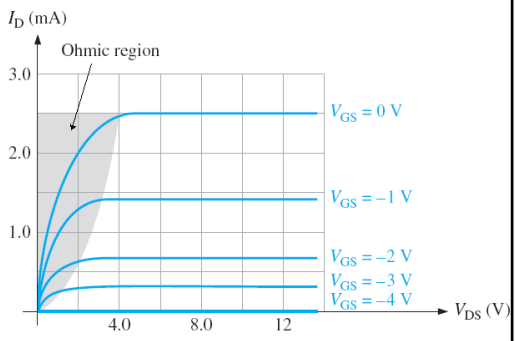
$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{9\text{ V} - 5\text{ V}}{10\text{ mA}} = \mathbf{400\ \Omega}$$



8-4: The Ohmic region

The **ohmic region** is the portion of the FET characteristic curves (shown in figure) in which Ohm's law can be applied. When ***properly biased in the ohmic region***, a JFET exhibits the properties of a variable resistance, where the value of resistance between drain and source (R_{DS}) is controlled by V_{GS}.

Biasing the JFET in the ohmic region (determining the dc load line that intersect the characteristic curve) can be done by setting the saturation drain current ($I_{D(sat)}$), where $I_{D(sat)} << I_{DSS}$ → the load line intersect most of the curves in the ohmic region



Ohmic region is the region extended from the origin to the active region (pinch off) of I_D characteristic curves

8-4: The Ohmic region

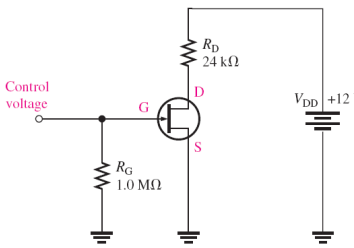
The dc load line in the ohmic region for given circuit can be drawn as follows:

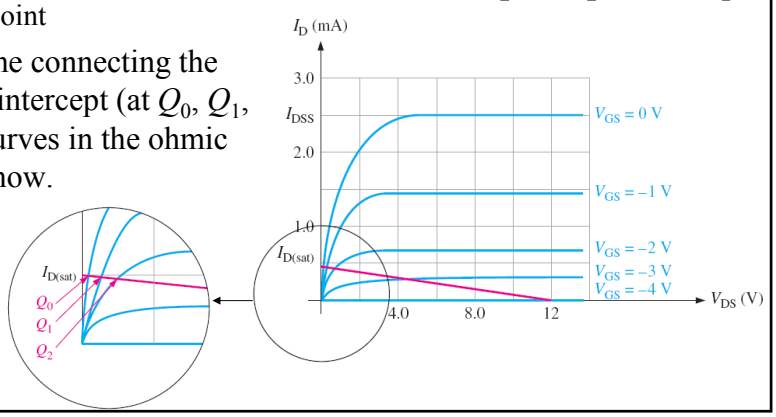
a) $I_{D(sat)} = \dfrac{V_{DD}}{R_D} = \dfrac{12\text{ V}}{24\text{ k}\Omega} = 0.50\text{ mA}$

This set the first point at $V_{DS} = 0$ and $I_{D(sat)}$

b) At $V_{DS} = V_{DD}$ when $I_D = 0$, we can set the second point

The load line connecting the two points intercept (at Q_0, Q_1, Q_2) most curves in the ohmic region as show.



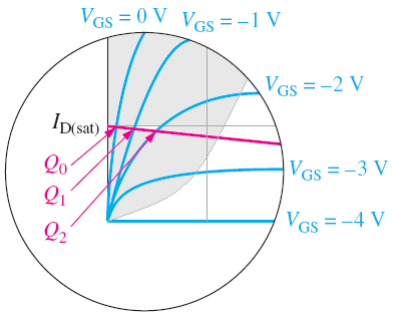


8-4: The Ohmic region

- the figure shows that The Q-point is moved along the load line by varying V_{GS} from 0 to -2

- At any point the resistance between the drain and source can be calculated from

$$R_{DS} = \frac{V_{DS}}{I_D}$$



- As expected, the figure shows that for less I_D we have more V_{DS}
→ R_{DS} increases with increasing V_{GS}

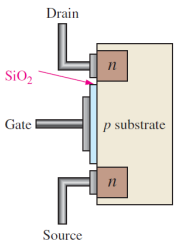
See example 8-14 for how R_{DS} highly varies with V_{GS}

8-5: The MOSFET

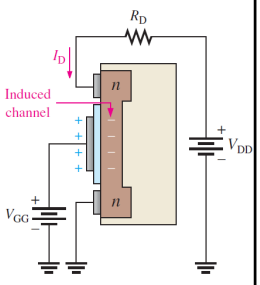
- The metal oxide semiconductor FET uses an insulated gate (layer of SiO_2) to isolate the gate from the channel. Two types are the enhancement mode (E-MOSFET) and the depletion mode (D-MOSFET).

E-MOSFET – Main Structure

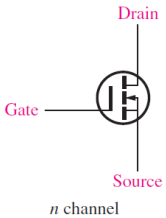
- E-MOSFET has no channel until it is induced by a voltage applied to the gate, so it operates only in enhancement mode. An *n*-channel type is illustrated here; a positive gate voltage above a threshold value induces the channel creating a thin layer of -ve charges (electrons). As V_{GS} increase → -ve charges increase → conductivity increase



(a) Basic construction



(b) Induced channel ($V_{GS} > V_{GS(th)}$)



n channel

8-5: The MOSFET

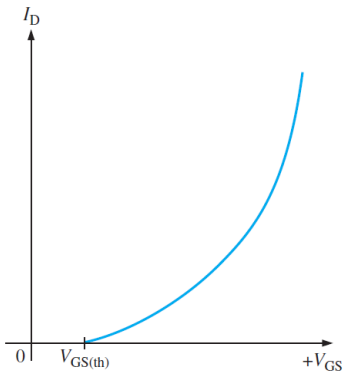
E-MOSFET – transfer characteristic curve

■ the general transfer characteristic curves for n-channel E-MOSFET shows that there is no drain current until reaching a threshold voltage, $V_{GS(th)}$.

The equation for the E-MOSFET transfer characteristic curve is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

Where K is constant depend on particular E-MOSFET (can be calculated from the equation or given in data sheet)



(a) *n* channel

8-5: The MOSFET

E-MOSFET – biasing

■ there are two ways to bias an E-MOSFET are voltage-divider bias, and drain-feedback bias. In E-MOSFET V_{GS} must be > $V_{GS(th)}$

For voltage divider bias

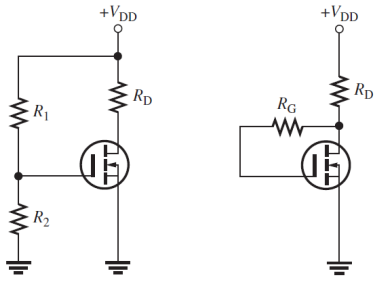
$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

where $I_D = K(V_{GS} - V_{GS(th)})^2$

Fro drain feedback bias, IG is negligible → no Voltage across R_G → $V_G = V_D$

$$V_{GS} = V_{DS}.$$



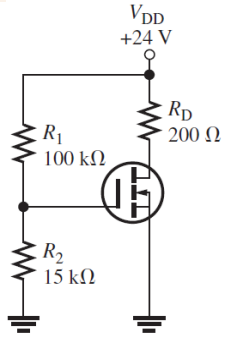
(a) Voltage-divider bias (b) Drain-feedback bias

8-5: The MOSFET

E-MOSFET : Example

Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Figure 8–47. Assume this particular MOSFET has minimum values of $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 2$ V.

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\,\text{k}\Omega}{115\,\text{k}\Omega}\right)24\,\text{V} = \mathbf{3.13\,V}$$



Now calculate I_D for $V_{GS} = 3.13$ V.

To calculate I_D wee need to find K → from given $I_{D(on)}$

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\,\text{mA}}{(4\,\text{V} - 2\,\text{V})^2} = 50\,\text{mA/V}^2$$

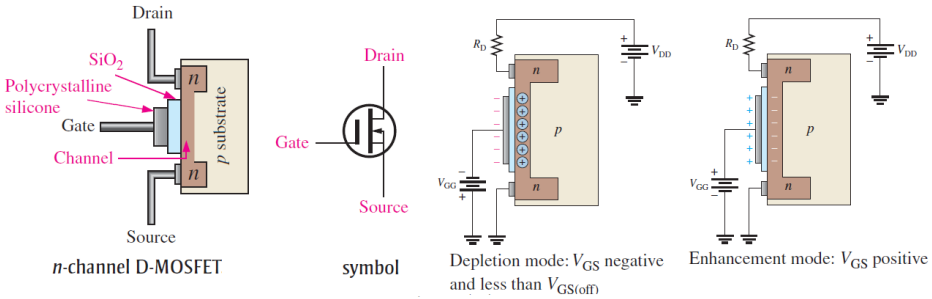
Hence I_D for $V_{GS} = 3.13$V is $I_D = K(V_{GS} - V_{GS(th)})^2 = (50\,\text{mA/V}^2)(3.13\,\text{V} - 2\,\text{V})^2 = 63.8\,\text{mA}$

→ $V_{DS} = V_{DD} - I_D R_D = 24\,\text{V} - (63.8\,\text{mA})(200\,\Omega) = \mathbf{11.2\,V}$

8-5: The MOSFET

D-MOSFET – Main Structure

■ The D-MOSFET has a channel that can is controlled by the gate voltage. For an *n*-channel type, a negative voltage depletes the channel (Depletion mode); and a positive voltage enhances the channel (Enhancement mode).



Here we will concentrate on Depletion mode MOSFET (D-MOSFET) because it is the most common used

8-5: The MOSFET

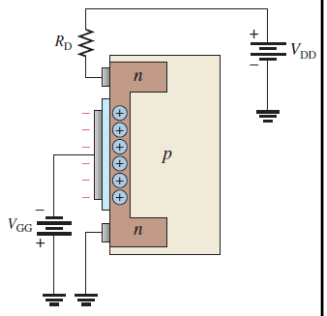
D-MOSFET

- In depletion mode, as V_{GS} increase → +ve ions in the channel increase → less electrons → conductivity decreases → Drain current decreases as shown in transfer curve

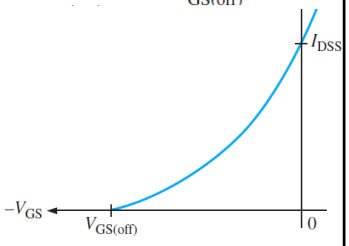
- D-MOSFET has same characteristics as JFET as you note from transfer curve where $V_{GS(off)} = -V_P$ and at $V_{GS} = 0$, $I_D = I_{DSS}$

Same drain current relation is also the same

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



Depletion mode: V_{GS} negative and less than $V_{GS(off)}$



n channel

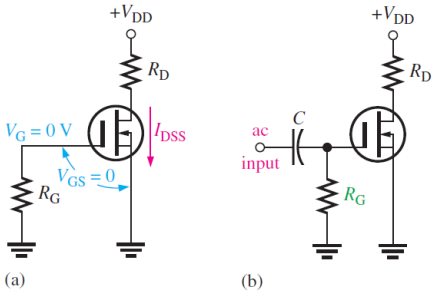
8-5: The MOSFET

D-MOSFET – biasing

In addition to biasing methods for E-MOSFET (voltage divider and drain feedback) D-MOSFETs can also be biased with zero biasing method shown (by setting $V_{GS} = 0$ → $I_D = I_{DSS}$). Hence

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

The purpose of R_G is to accommodate an ac signal input by isolating it from ground



Example: calculate V_{DS} if $R_D = 620\Omega$, $R_G = 10M\Omega$, $V_{DD} = +18V$, $V_{GS\,(off)} = -8V$, and $I_{DSS} = 12mA$

since $I_D = I_{DSS} = 12$ mA

→ $V_{DS} = V_{DD} - I_{DSS}R_D = 18\text{ V} - (12\text{ mA})(620\ \Omega) =$ **10.6 V**